Attorney's Docket No. 9180-5 PATENT

#6/Declaration
5/27/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: J. Daniel Mis et al.
Application No.: 09/966,316
Filing Date: September 27, 2001
For: METHODS OF FORMING METALLURGY STRUCTURES FOR WIRE AND SOLDER BONDING AND RELATED STRUCTURES

Examiner: W.C. Vesperman
Group Art Unit: 2813

Assistant Commissioner for Patents
Washington, DC 20231

DECLARATION OF MR. J. DANIEL MIS PURSUANT TO 37 C.F.R. 1.131

Sir:

I, J. Daniel Mis, hereby declare and say that:

1. I am an inventor of the subject matter of the rejected claims.

2. Prior to January 19, 2001, the named inventors conceived providing first and second metallurgy structures on the respective first and second input/output pads, the first and second metallurgy structures having a shared metallurgy structure adapted to receive solder and wire bonds. Prior to January 19, 2001, the named inventors also conceived providing an underbump metallurgy layer on an input/output pad, providing a barrier layer on the underbump metallurgy layer, and providing a passivation layer on a barrier layer. Prior to January 19, 2001, the named inventors further conceived providing first and second barrier layers on the respective first and second input/output pads wherein the first and second barrier layers each comprise nickel; providing first and second passivation layers on the respective first and second barrier layers, and providing a solder structure on the first passivation layer while maintaining the second passivation free of solder. Prior to January 19, 2001, the named inventors also conceived forming an input/output pad on a substrate, and forming a bonding structure on the input/output pad, the bonding structure including a barrier layer comprising nickel on the input/output pad, and a solder structure on the barrier layer.

3. In support of the above statement of Section 2, I hereby submit as **Appendix A** a copy of a Disclosure entitled "A process for Chip Scale Packaging Including the Integration of Wire Bonding and Solder Deposition on the Same Chip" submitted by Kevin Engel and J. Daniel Mis. The dates within this document have been blocked out, but are before January 19, 2001.

4. Due diligence was exercised from prior to January 19, 2001, to the filing of the above referenced patent application.

5. In support of the above statement of Section 4, I hereby submit as **Appendix B** a copy of a letter dated November 8, 2000, confirming that Myers Bigel Sibley and Sajovec, P.A. would prepare an application relating to "A Process For Chip Scale Packaging Including The Integration Of Wire Bonding And Solder Deposition On The Same Chip"; as **Appendix C** a copy of a letter from Myers Bigel Sibley & Sajovec, P.A. dated May 2, 2001, forwarding an initial draft of a patent application for inventor review; as **Appendix D** a copy of a letter dated May 17, 2001, forwarding formal drawings; as **Appendix E** a copy of a letter dated July 11, 2001, forwarding a revised final draft of the patent application; as **Appendix F** a copy of an e-mail dated August 8, 2001, stating that the draft application was not received and that it was being resent; and as **Appendix G** a copy of an e-mail dated August 9, 2001, indicating that the inventor was out of town. The Application was filed on September 27, 2001.

6. In summary, my statements herein and the documents I have concurrently submitted show conception of the invention prior to January 19, 2001, coupled with due diligence from prior to January 19, 2001, to the filing of the application on September 27, 2001.

7. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true. I further declare that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful

false statements may jeopardize the validity of the application or any patent issued thereon.

J. Daniel Mis 5/5/03

J. Daniel Mis Date

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Application No.: 09/966,316 Group Art Unit: 2813
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For: METHODS OF FORMING METALLURGY STRUCTURES FOR WIRE AND SOLDER BONDING AND RELATED STRUCTURES

Assistant Commissioner for Patents
Washington, DC 20231

DECLARATION OF MR. KEVIN ENGEL
PURSUANT TO 37 C.F.R. 1.131

Sir:

I, Kevin Engel, hereby declare and say that:

1. I am an inventor of the subject matter of the rejected claims.

2. Prior to January 19, 2001, the named inventors conceived providing first and second metallurgy structures on the respective first and second input/output pads, the first and second metallurgy structures having a shared metallurgy structure adapted to receive solder and wire bonds. Prior to January 19, 2001, the named inventors also conceived providing an underbump metallurgy layer on an input/output pad, providing a barrier layer on the underbump metallurgy layer, and providing a passivation layer on a barrier layer. Prior to January 19, 2001, the named inventors further conceived providing first and second barrier layers on the respective first and second input/output pads wherein the first and second barrier layers each comprise nickel; providing first and second passivation layers on the respective first and second barrier layers, and providing a solder structure on the first passivation layer while maintaining the second passivation free of solder. Prior to January 19, 2001, the named inventors also conceived forming an input/output pad on a substrate, and forming a bonding structure on the input/output pad, the bonding structure including a barrier layer comprising nickel on the input/output pad, and a solder structure on the barrier layer.

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false statements may jeopardize the validity of the application or any patent issued thereon.

Kevin Engel

5/5/03
Date